Specifications

Version 01.00

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I/Q Modulation Generator R&S®AFQ 100A

Specifications

ROHDE&SCHWARZ

CONTENTS

KEY FEATURES

Broad scope of applications

- Variable memory clock rate (1 kHz to 300 MHz) can be optimally adjusted to the useful signal
- Maximum I/Q bandwidth of up to 100 MHz for an RF bandwidth of 200 MHz
- Long signal duration at 256 Msamples or 1 Gsample
- Analog I/Q outputs (balanced and unbalanced) and optional digital outputs
- Variable output level at the analog outputs
- Multisegment waveform reduces switching time between different signals, no reloading required
- Optimum memory use due to integrated clock rate converter and memory granularity of 1
- Shiftable markers without disrupting and recalculating the output signal

Outstanding signal quality

- Excellent SFDR of typ. 83 dBc (1 MHz signal at 100 MHz bandwidth)
- Frequency response across 100 MHz, I/Q bandwidth typ. 0.05 dB
- Versatile impairments
  - Settable skew with 10 ps resolution to allow exact adjustment of different cable lengths
  - Gain and offset for I and Q can be set independently
  - Phase error
- Loadable precorrection to compensate for external components such as I/Q modulators (minimum frequency response across all components involved)
- Adjustment of DC offsets by biasing the differential I/Q outputs

Connectors and operation

- Remote control via GPIB, USB and LAN
- User interface via external monitor or Windows Remote Desktop
- R&S WinIQSIM2 for controlling the R&S AFQ100A and generating test signals in line with different standards
- Direct control via MATLAB®
- USB connectors for USB equipment (keyboard, mouse, memory stick)

Specifications

Specifications apply under the following conditions:

30 minutes warm-up time at ambient temperature, specified environmental conditions met, calibration cycle adhered to, and total calibration performed. Data designated “overrange“ or “underrange” and data without tolerance limits is not binding.

EMC specifications are tested with sufficiently shielded cables and accessories (e.g. mouse and keypad, double-shielded cables for I and Q, rear BNC connectors). To prevent degradation of these specifications, appropriate equipment must be used.

Output memory

Waveform length (data and markers)		from 3 samples in steps of 1 sample
	waveform memory (R&S AFQ-B10)	up to 256 Msamples
	waveform memory (R&S AFQ-B11)	up to 1 Gsample
Memory clock		1 kHz to 300 MHz
Waveform bandwidth		max. 0.33 × memory clock
Amplitude resolution of data words		16 bit analog and digital (R&S AFQ-B18)
Marker channels		4
	control by separate signal generators from main memory	 pulse, pattern, on/off ratio 4 bits per sample, deducted from waveform memory
	offset relative to signal waveform	0 samples to 4000 samples

Clock generation

Clock rates, analog output	memory clock	1 kHz to 300 MHz
	converter clock (with digital lowpass filter and clock rate converter)	1200 MHz
Clock rates, digital output, port 1 (LVDS, multiplexed × 7)	interface clock (with digital lowpass filter and clock rate converter)	100 MHz
	data clock	700 MHz (according to TIA644)
	memory clock	1 kHz to interface clock rate
	operating modes with clock rate converter with data enable	 with digital lowpass filter and clock rate conversion (memory clock to interface clock), configurable filter for frequency response correction valid samples are marked with a "data valid" bit; system clock rate = memory clock
Clock rates, digital output, port 2 (LVDS, parallel)	interface clock	1 kHz to 300 MHz
	data clock	same as interface clock (direct output, no filters)
	memory clock	same as interface clock
Resolution		1×10^{-7}
Output		memory clock
	level	LVTTL, 2 V into 50 Ω
Input	input level	0 V to 3 V, threshold can be set between 10 mV and 1.9 V
	input impedance	50 Ω/1 kΩ, switchable
	frequency	1 kHz to 150 MHz

Reference frequency

Output for internal reference	frequency	10 MHz
	aging (after 30 days of operation)	1×10^{-6}/year
	temperature effect (+5 °C to +45 °C)	1×10^{-6}
	level	0.5 V (rms, sinewave, into 50 Ω)
	output impedance	50 Ω
Input for external reference	frequency	10 MHz
	permissible frequency deviation	0.05 %
	level	0.1 V to 2 V (rms, sinewave)
	input impedance	50 Ω

Signal output

Number of outputs		2 (I and Q), each switchable between balanced and unbalanced
Output (unbalanced)		1 V pp (into 50 Ω (nominal))
	level range	0 V to 1.5 V pp (into 50 Ω)
	hardware attenuator	0 dB to 21 dB in steps of 3 dB
	fine variation	±5 %, separately for I and Q channel
	resolution	14 bit
	impedance	50 Ω each
	level error (DC, at 1 V pp)	<±1 % (at 1 kHz, after auto alignment)
	level difference between the two channels	<±0.1 % (at 1 kHz, after auto alignment)
	frequency response (relative to DC)	±0.05 dB up to 50 MHz ±0.1 dB up to 100 MHz
Output (balanced)		2 V pp (between I and $\bar{I}$ into 100 Ω, nominal)
	level range	0 V to 3 V pp (into 100 Ω)
	hardware attenuator	0 dB to 21 dB in steps of 3 dB
	fine variation	±5 %, separately for I and Q channel
	resolution	14 bit
	impedance	50 Ω each
	bias voltage	–2.5 V to +2.5 V in steps of 10 mV
	level error (DC, at 2 V pp)	<±1 % (at 1 kHz, after auto alignment)
	level difference between the two channels	<±0.1 % (at 1 kHz, after auto alignment, bias voltage off) <±0.5 % (at 1 kHz, after auto alignment, bias voltage on)
Spectral purity	SFDR (without harmonics)	>80 dBc, typ. 83 dBc
	harmonics	
	10 MHz signal (bandwidth 0 Hz to 100 MHz, V_{out} = 1 V pp, bias voltage off)	<–70 dBc, typ. –75 dBc
	50 MHz signal (bandwidth 0 Hz to 500 MHz, V_{out} = 1 V pp, bias voltage off)	<–65 dBc, typ. –68 dBc
	100 MHz signal (bandwidth 0 Hz to 500 MHz, V_{out} = 1 V pp, bias voltage off)	typ. –50 dBc
	3GPP signal, test model 1/64 (V_{out} = 1.5 V pp, bias voltage off)[1] adjacent channel alternate channel	 typ. –80 dBc typ. –80 dBc
	3GPP signal, test model 1/64 (V_{out} = 1.5 V pp, bias voltage off, f(IF) = 25 MHz) adjacent channel alternate channel	 typ. –75 dBc typ. –77 dBc
Noise floor (at V_{pp} = 1.5 V)		–154 dBc (1 Hz)
Digital filters		4 filters (15 taps each) in butterfly structure
Skew between I and Q channel		–2 ns to +2 ns (can be digitally set in steps of 10 ps)
DC offset	alignment	automatic, separately for each channel
	residual offset	<±1 mV (after auto alignment)

[1] Measured with additional external channel filter.

Operating modes

Continuous output		repetitive output of waveform from output memory
Single output		single output of waveform from output memory
Segment mode		output of up to 2048 different segments; for each segment, the stepping condition for advancing to the next segment (NEXT) can be selected
Trigger inputs		2, TRIG and NEXT (BNC)
	input level	0 V to 3 V, threshold can be set between 10 mV and 1.9 V
	input impedance	50 Ω/1 kΩ, switchable
	pulse width	min. 10 ns
	min. trigger repetition period	100 µs + 25 memory clock cycles
	dead time between trigger input and output of first data word	1.8 µs + 13 memory clock cycles + 3.3 ns jitter; with an external trigger, the output is synchronized with the trigger input
Direct IF		digital modulator for direct generation of user-selectable IF (within signal bandwidth)

Auxiliary outputs

Markers		user-configurable signals aligned to data words
	number	4, BNC
	level	LVTTL, 2 V into 50 Ω

BERT (option R&S AFQ-K80)

Data supplied by the DUT can be compared with a pseudo-random binary sequence (= data content of the I/Q signal) output by the instrument. Results are transferred to the host computer (via the currently used remote control system).		
Pseudo-random binary sequences		PRBS9, PRBS11, PRBS15, PRBS16, PRBS20, PRBS21, PRBS23
Clock source		clock signal supplied by DUT; one clock pulse is required for each valid bit
Clock rate		min. 1 kHz, max. 100 MHz
Interface		BNC
	data	TTL
	clock	TTL
	setup time	4 ns
	hold time	0 ns
Polarity		normal and inverted (data, clock)
	input level	0 V to 3 V, selectable threshold
	input impedance	50 Ω/1 kΩ, switchable
Results		BER in ppm

Digital outputs (option R&S AFQ-B18)

Output	port 1	multiplexed I/Q data stream, compatible with other Rohde & Schwarz equipment
	port 2	parallel I/Q interface
Port 1	operating modes interpolated with enable	 memory data with digital lowpass filter and clock rate converter (conversion to interface clock) valid samples are marked with a "data valid" bit in the data stream
	clock source	external, internal
	interface	26-pin I/Q interface
	data	LVDS
	clock	LVDS
Port 2	operating mode	direct output of memory data
	clock source	external, internal
	interface	68-pin HD-SCSI, 16 bit for each I and Q, 2 data clock lines
	data	LVDS, >±200 mV into 100 Ω
	clock	LVDS, >±200 mV into 100 Ω
	skew	200 ps
	rise time	400 ps

General data

Computer

Computer		industrial PC
Mass memory		3.5" SATA hard disk drive, 160 Gbyte
Interfaces		USB 2.0 (master and slave), Gigabit Ethernet, IEC 625 (IEEE 488)
Operating software updates		via USB

Remote control

		via USB, Ethernet, IEC 625-2 (IEEE 488)
Command set		SCPI 1996.0 with extensions
IEC/IEEE interface functions		SH1, AH1, T6, L4, SR1, RL1, PP1, DC1, DT1, C0

Operating data

Power supply		100 V to 240 V AC, 50 Hz to 60 Hz, 2.0 A to 1.0 A
	power factor correction	meets EN 61000-3-2
	EMC	meets EN 55011 class B, EN 61326
Electromagnetic compatibility		meets EN 50081-1 and EN 50082-1 (EMC Directive of EU)
	immunity to RFI	10 V/m
Environmental conditions		
	operating temperature range	+5 °C to +45 °C; meets IEC 68-2-1 and IEC 68-2-2
	storage temperature range	–40 °C to +70 °C
	climatic stress damp heat	95 % relative humidity at +40 °C; meets IEC 68-2-1, without condensation
Mechanical resistance	vibration, sinusoidal	5 Hz to 150 Hz, max. 2 g at 55 Hz, max. 0.5 g at 55 Hz to 150 Hz, meets EN 60068-2-6
	vibration, random	10 Hz to 300 Hz, acceleration 1.2 g (rms) meets EN 60068-2-64
	shock	40 g shock spectrum, meets EN 60068-2-27, MIL-STD-810E
Electrical safety		meets IEC 1010-1, EN 61010-1, UL 61010-1, CAN/CSA-C22.2 No. 61010-1-04
Approvals		VDE-GS, $_{C}$CSA$_{US}$
Dimensions	W × H × D	426.7 mm × 87.6 mm × 450 mm
Weight	when fully equipped	7.5 kg
Warranty period		1 year
Recommended calibration interval		3 years

Ordering information

Designation	Type	Order No.
I/Q Modulation Generator[2]	R&S AFQ100A	1401.3003.02
Including power cable, Quick Start Guide and CD-ROM (with operating and service manual)		
Options		
Baseband hardware		
Waveform Memory 256 Msample	R&S AFQ-B10	1401.5106.02
Waveform Memory 1 Gsample	R&S AFQ-B11	1401.5206.02
Digital I/Q Output	R&S AFQ-B18	1401.5306.02
Baseband software		
Bit Error Ratio Tester	R&S AFQ-K80	1401.5006.02
R&S WinIQSIM2 options		
Digital Standard GSM/EDGE	R&S AFQ-K240	1401.6302.02
Digital Standard 3GPP FDD	R&S AFQ-K242	1401.6354.02
Digital Standard 3GPP FDD Enhanced MS/BS Tests, incl. HSDPA	R&S AFQ-K243	1401.6402.02
Digital Standard GPS	R&S AFQ-K244	1401.6454.02
Digital Standard HSUPA	R&S AFQ-K245	1401.6504.02
Digital Standard CDMA2000® incl. 1xEV-DV	R&S AFQ-K246	1401.6554.02
Digital Standard IEEE 802.11 (a/b/g)	R&S AFQ-K248	1401.6602.02
Digital Standard IEEE 802.16	R&S AFQ-K249	1401.6654.02
Digital Standard TD-SCDMA	R&S AFQ-K250	1401.6702.02
TD-SCDMA Enhanced	R&S AFQ-K251	1401.6754.02
Multicarrier CW Signal Generation	R&S AFQ-K261	1401.6802.02
Additive White Gaussian Noise	R&S AFQ-K262	1401.6854.02
Recommended extras		
Hardcopy manuals (in English, UK)		1401.3084.32
Hardcopy manuals (in English, US)		1401.3084.39
19“ Rack Adapter	R&S ZZA-211	1096.3260.00
Keyboard with USB Interface (US characteristic set)	R&S PSL-Z2	1157.6870.04
Mouse with USB Interface, optical	R&S PSL-Z10	1157.7060.03
External USB DVD Drive	R&S PSP-B6	1134.8201.22

[2] The base unit must be ordered together with an R&S AFQ-B10 or R&S AFQ-B11 option.

Certified Quality System
ISO 9001
DQS REG. NO 1954 QM

Certified Environmental System
ISO 14001
DQS REG. NO 1954 UM

For product brochure, see PD 5213.6541.12
and www.rohde-schwarz.com
(search term: AFQ100A)

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